

NITED STATES PATENT AND TRADEMARK OFFICE PATENT TRANSMITTAL FORM

Serial No.:

For:

Boppana et al.

10/079,809

DIGITAL LOGIC CIRCUITS USED TO DESIGN INTEGRATED TO TROUTS

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Filed:

Group Art Unit:

Confirmation No.:

2344

Examiner:

Not yet assigned

Attorney Docket No.:

162.7287USU

COMMISSIONER FOR PATENTS Washington, D.C. 20231

Dear Sir:

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DEC 1 6 2002

Transmitted herewith is:

Information Disclosure Statement; 1.

Technology Center 2600

- 2. PTO Form 1449 with copy of citations;
- Transmittal letter in duplicate; and 3.
- Postcard.

Please charge any additional fees or credit any such fees, if necessary to Deposit Account No. 01-0467 in the name of Ohlandt, Greeley, Ruggiero & Perle. A duplicate copy of this sheet is attached.

Respectfully submitted,

December 3, 2002

Date

Paul D. Greeley, Esq.

Reg. No. 31,019

Ohlandt, Greeley, Ruggiero & Perle, L.L.P.

One Landmark Square, 10th Floor Stamford, Connecticut 06901-2682

(203) 327-4500

CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231, ON DECEMBER 3, 2002.

Kenroy A. Browne **NAME**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE OFC 11 2002

Tomana et al.

Applicants:

Serial No

For:

DIGITAL LOGIC CIRCUITS USED TO DESIGN INTEGRATED CIRCUITS

Filed:

February 15, 2002

Group Art Unit:

2825

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DEC 1 6 2002

Confirmation No.:

2344

Technology Center 2600

Examiner:

Not yet assigned

Attorney Docket No.:

162.7287USU

Commissioner for Patents Washington, D.C. 20231

C.F.R. §1.17(p);

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In accordance with applicants' duty of disclosure under 37 C.F.R. §1.56, please find attached hereto form PTO-1449 listing information which may be material to the patentability of this application, filed on February 15, 2002. This Information Disclosure Statement is being

filed:	
	Within three (3) months of the filing date of the national application;
	Within three (3) months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application;
<u>XXX</u>	Before the mailing date of a first Office Action on the merits;
	After the filing date or date of first Office Action, but before the mailing date of a final action under 37 C.F.R. §1.113, provided that this occurs prior to the issuance of a Notice of Allowance and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e) or the fee set forth in 37 C.F.R. §1.17(p);
	After the filing date or date of first Office Action, but before the mailing date of a Notice of Allowance under 37 C.F.R. §1.311, provided that this occurs prior to the final action and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e) or the fee set forth in 37

 After the mailing date of a final action under 37 C.F.R. §1.113, provided that this occurs prior to the issuance of a Notice of Allowance and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e), a petition requesting consideration of the I.D.S., and the petition fee set forth in 37 C.F.R. §1.17(i)(1); and
 After the mailing date of a Notice of Allowance under 37 C.F.R. §1.311, provided that this occurs prior to the issuance of a final action and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e), a petition requesting consideration of the I.D.S., and the petition fee set

It should be understood that attention has been called to the references that have been deemed to be pertinent to the claimed present invention. In concluding what was pertinent, the criteria employed was considered most appropriate in light of the invention shown in the present application. However, the Examiner or others may deem some other criteria to be just as appropriate or more appropriate. Therefore, the Examiner is respectfully urged to review the listed references and to make the usual careful independent search for other prior art that may be pertinent.

Respectfully submitted,

<u>December 3, 2002</u>

Date

forth in 37 C.F.R. §1.17(I)(1).

Paul D. Greeley

Reg. No. 31,019

Ohlandt, Greeley, Ruggiero & Perle, L.L.P.

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Sheet 1 of 1

FORM PTO-1449			Docket Number (Opti	Docket Number (Optional) Application Number						
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IN AN APPLICATION			Applicant	Applicant						
			Boppana et al.							
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·····	OTHE	R DOCUMENTS	(including Author Title Date	Pertinent Pages	Etc.)					
	OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.) Kazuo Taki, "A Survey for Pass-Transistor Logic Technologies", IEEE, 1998.									
	Mineo Kaneko and Jialin Tian, "Concurrent Cell Generation and Mapping for CMOS Logic Circuits", IEEE, 1997.									
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EVALUED	<u> </u>	-	DATE CONSIDERED							
EXAMINER										